WHAT IS CLAIMED IS

1. A transistor comprising:

a P-substrate;

a first diffusion region and a second diffusion region having N conductivity-type ions formed in said P-substrate, wherein said first diffusion region comprises an extended drain region;

a drain diffusion region containing N+ conductivity-type ions, forming a drain region in said extended drain region;

a plurality of P-field blocks formed in said extended drain region; wherein said P-field blocks have different sizes; wherein a smallest size P-field block is located nearest to said drain region; wherein said P-filed blocks are used for generating junction fields;

a source diffusion region having N+ conductivity-type ions, forming a source region in said N-well formed by said second diffusion region, wherein a largest size P-field block is located nearest to said source region;

a channel, formed between said drain region and said source region;

a polysilicon gate electrode, formed over said channel to control a current flow in said conduction channel;

a contact diffusion region containing P+ conductivity-type ions, forming a contact region in said N-well formed by said second diffusion region; and

an isolated P-well formed in said N-well formed by said second diffusion region for preventing from breakdown; wherein said isolated P-well formed in said second diffusion region encloses said source region and said contact region.

2. The transistor of claim **1**, wherein said N-well formed by said second diffusion region produces a low-impedance path for said source region, and restricts said current

flow in between said drain region and said source region.

3. The transistor of claim **1** further comprising:

a thin gate oxide and a thick field oxide, formed in underneath said polysilicon gate electrode.

a drain-gap, formed between said drain diffusion region and said thick field oxide to maintain a space between said drain diffusion region and said thick field oxide; and

a source-gap, formed between said thick field oxide and said isolated P-well to maintain a space between said thick field oxide and said isolated P-well, wherein said drain-gap and said source-gap are used to increase breakdown voltage, wherein said drain-gap further reduces an on-resistance of said channel.

4. The transistor of claim **1**, further comprising a silicon dioxide insulation layer, covering said polysilicon gate electrode and said thick field oxide;

5. The transistor of claim **1**, further comprising:

a source metal contact having a first metal electrode, for contacting with said source diffusion region and said contact diffusion region; and

a drain metal contact, having a second metal electrode, for contacting with said drain diffusion region.

6. The transistor of claim **1**, further comprising:

a drain bonding pad, connected to said drain metal contact for a drain electrode;

a source bonding pad, connected to said source metal contact for a source electrode; and

a gate bonding pad, connected to said polysilicon gate electrode.

7. The LDMOS transistor of claim **1**, wherein said P-field blocks are formed in said extended drain region of said N-well, wherein said N-well and said P-field blocks deplete

a drift region and equalize the capacitance of parasitic capacitors between said drain region and said source region, and decrease the on-resistance of said channel.